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10/775,523	02/09/2004	Sam Nemazie	SiliconStor-03US	1041

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Maryam Imam. Esq.
LAW OFFICES OF IMAM
Suite 1010
111 North Market St.
San Jose, CA 95113

EXAMINER	
LEE, CHUN KUAN	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/775,523	NEMAZIE, SAM	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-20 have been considered but are moot in view of the new ground(s) of rejection. Claim objection of claim 13 and claim rejection of claim 8 under 35 U.S.C. 112 are withdrawn. Currently claims 1-20 are pending for examination.

2. In responding to applicant's argument that Garieff fails to teach claim 1's claimed limitation that "wherein the FIS of the first and second host and the device Identify which one of the first or second host units is an origin and/or destination host so...", as stated on page 12, last paragraph. Applicant's argument has fully been considered, but is found not to be persuasive.

The identification of which one of the first host unit or the second host unit is the origin and/or destination host is implemented by utilizing the FIS' tag information, as when the host sends the FIS with the tag information to the device, the tag information is stored as OldTag and a NewTag is assigned before sending the FIS to the device and when the device finish processing the FIS and transfer the data back to the corresponding host, the tag information from the device is replaced with the OldTag from the original FIS, therefore able to properly route to the correct host (col. 10, ll. 27-64 and col. 12, ll. 23-27).

Claim Objections

Claims 1, 9 and 14 are objected to because of the following informalities:

in claim 1, line 12, "accepting commands" should be replace with -accepting FIS-;

in claim 9, line 12, "accepting commands" should be replace with -accepting FIS-; and

in claim 15, line 13, "accepting commands" should be replace with -accepting FIS-. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7 and 9-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Grieff et al. (US Patent 6,961,813) in view of Talati (US Patent 6,763,402).

4. As per claims 1, 9 and 14, Grieff teaches a switch coupled between a plurality of host units and a device via serial advanced technology attachment (SATA) links, for routing frame information there between the first and the second host units and the device, said switch comprising:

a. a first SATA port (H0_Link Layer 130 of Fig. 1), capable of receiving a frame information structure (FIS) coupled to a first host unit (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);

b. a second SATA port (H1_Link Layer 132 of Fig. 1), capable of receiving a FIS, coupled to a second host unit (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);

c. a third SATA port (Device-Side Link Layer of Fig. 1), capable of receiving a FIS, coupled to a device (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56); and

d. an arbitration and control circuit (switch 110 and arbiter module 112 of Fig. 1) for selecting one of the first host or second host units to be coupled to the device, through the switch, and further wherein the FIS of the first and second host units and the device identify which one of the first or second host units is an origin and/or destination host so that routing of FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34; col. 5, l. 17 to col. 6, l. 56; col. 10, ll. 27-64 and col. 12, ll. 23-27)

Grieff does not expressly teach the switch coupled between the plurality of host units and the device via SATA links, for routing frame information there between the first and the second host units and the device, said switch comprising:

selecting one of the first host or the second host units to concurrently access the device by accepting FIS, from either of the first or the second host units, at any given time, including when the deice is not in an idle state; and

wherein while one of the first or second host units is coupled to the device, through the switch, the other one of the first or second host units sends the FIS to the switch for routing to the device.

Talati teaches a system and a method comprising two or more hosts to simultaneous concurrent access the same data storage device by buffering any access request to the data storage device in a queue while said data storage device is busy responding to a prior access and responded to the buffered access request later (col. 2, ll. 14-26).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Talati's queuing of access request into Grieff's arbitration and control circuit. The resulting combination of the references further teaches the switch coupled between the plurality of host units and the device via SATA links, for routing frame information there between the first and the second host units and the device, said switch comprising:

the first host unit and the second host unit to simultaneous concurrent access the device by buffering any FIS received from either of the first host unit and the second host unit in the queue if the device is currently busy responding to the previous FIS, therefore able to accept the FIS at any given time; and

wherein while the device is busy with the FIS from one of the first host unit or the second host unit, the other one of the first host unit or the second host unit sends the FIS to the switch to be buffered in the queue and routed to the device later.

Therefore, it would have been obvious to combine Talati with Grieff for the benefit of preventing chaos that might occur in performing the concurrent access to the same storage device (Talati, col. 2, ll. 27-37).

5. As per claims 2, 11 and 16, Grieff and Talati teach all the limitations of claims 1, 9 and 14 as discussed above, where Grieff further teaches said switch comprising wherein said device is a storage unit (Grieff, col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 15, ll. 9-22).

6. As per claims 3, 12 and 17, Grieff and Talati teach all the limitations of claims 1, 9 and 14 as discussed above, where Grieff further teaches said switch comprising wherein said switch is employed in an enterprise system (Grieff, col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 15, ll. 9-22).

7. As per claims 4, 13 and 18, Grieff and Talati teach all the limitations of claims 1, 9 and 14 as discussed above, where Talati further teaches said switch comprising wherein said arbitration and control causes concurrent access of the device by the first and the second host units (Talati, col. 1, l. 7 to col. 2, l. 36)

8. As per claim 5, Grieff and Talati teach all the limitations of claim 1 as discussed above, where Grieff further teaches said switch comprising wherein a bit is used to indicate which host is the origin or destination of the FIS (Grieff, col. 4, ll. 47-57 and col. 10, l. 27 to col. 12, l. 29), as each FIS comprise an associated 5-bit tag utilized for identifying which host is the origin or the destination of the FIS.

9. As per claim 6, Grieff and Talati teach all the limitations of claim 1 as discussed above, where Grieff further teaches said switch comprising wherein said first, second and third ports are layer 2 ports (link layer ports) (Grieff, Fig. 1).

10. As per claims 7 and 10, Grieff and Talati teach all the limitations of claims 1 and 9 as discussed above, where Grieff further teaches said switch comprising wherein the switch provides for `route aware` routing (Grieff, col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34; col. 5, l. 17 to col. 6, l. 56 and col. 12, l. 60 to col. 14, l. 21), as FIS are properly routed between one of the associated hosts and the device.

11. As per claim 15, Grieff and Talati teach all the limitations of claim 14 as discussed above, where Grieff further teaches said switch comprising wherein the switch is a serial ATA switch (Grieff, col. 5, ll. 17-21).

12. As per claim 19, Grieff teaches a method for communication between multiple host units and a device, through a serial advanced technology attachment (ATA) switch

coupled to the multiple host units and the device using serial ATA links routing frame information therebetween, comprising:

a. receiving a frame information structure (FIS) through a first serial ATA port (H0_Link Layer 130 of Fig. 1), from to a first host unit (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);

b. receiving a FIS, through a second serial ATA port (H1_Link Layer 132 of Fig. 1), from a second host unit (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);

c. receiving a FIS through a third SATA port (Disk-Side Link Layer of Fig 1) (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);

d. arbitrating (arbitrate utilizing the arbiter module 112 of Fig. 1) between the first and second host units and the device (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);

e. selecting one of the first or second host units for coupling to the device through the switch when either of the first or second host units sends commands for execution by the device (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56);

f. coupling the device to the selected one of the first or second host units (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34 and col. 5, l. 17 to col. 6, l. 56); and

the FIS of the first and second host units and the device identifying which one of the first or second host units is an origin and/or destination host so that routing of FIS is transparent to the switch thereby reducing the complexity of the design of the switch

rendering its manufacturing less expensive (col. 2, l. 53 to col. 3, l. 45; col. 4, ll. 5-34; col. 5, l. 17 to col. 6, l. 56; col. 10, ll. 27-64 and col. 12, ll. 23-27).

Grieff does not teach the method for communication between multiple host units and the device comprising:

while the selected one of the first or second host units is coupled to the device, the other one of the first or second host units sending FIS to the switch for routing to the device

Talati teaches a system and a method comprising two or more hosts to simultaneous concurrent access the same data storage device by buffering any access request to the data storage device in a queue while said data storage device is busy responding to a prior access and responded to the buffered access request later (col. 2, ll. 14-26).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Talati's queuing of access request into Grieff's switch. The resulting combination of the references further teaches the method for communication between multiple host units and the device comprising:

while the device is busy with the FIS from one of the first host unit or the second host unit, the other one of the first host unit or the second host unit sends the FIS to the switch to be buffered and routed to the device later.

Therefore, it would have been obvious to combine Talati with Grieff for the benefit of preventing chaos that might occur in performing the concurrent access to the same storage device (Talati, col. 2, ll. 27-37).

13. As per claim 20, Grieff and Talati teach all the limitations of claim 19 as discussed above, where Grieff further teaches the method comprising wherein the steps of transmitting a frame information structure (FIS) through the first serial ATA port, transmitting a frame information structure (FIS) through the second serial ATA port, and transmitting a frame information structure (FIS) through the third serial ATA port (Grieff, col. 4, ll. 5-34 and col. 10, l. 27 to col. 12, l. 29), wherein the FIS is transmitted from the host-side through either the first or the second serial ATA ports and from the device through the third serial ATA port.

14. Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Grieff et al. (US Patent 6,961,813) and Talati (US Patent 6,763,402), and further in view of Kreifels (US Patent 4,891,788).

Grieff and Talati teach all the limitations of claim 1 as discussed above.

Grieff and Talati does not expressly teach said switch comprising a dual ported first-in-first-out (FIFO).

Kreifels teaches a system and a method comprising a dual port FIFO (Fig. 1).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Kreifels' dual port FIFO into Grieff and Talati's switch's inbound buffers. The resulting combination of the references teaches the switch further comprising the utilization of dual port FIFO as inbound buffers.

Therefore, it would have been obvious to combine Kreifels with Grieff and Talati for the benefit of enabling the read and write operation of the inbound buffer to be independent of each other (Kreifels, col. 1, l. 15 to col. 2, l. 6).

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

C.K.L.
08/30/2006

KIM HUYNH
SUPERVISORY PATENT EXAMINER
9/1/06